HACETTEPE UNIVERSITY

DEPARTMENT OF ELECTRICIAL AND ELECTRONICS ENGINEERING

GRADUATION PROJECT

DESIGN OF A COMPACT IMAGE CAPTURING DEVICE WITH FPGA

PROF. DR. ALİ ZİYA ALKAR

BEDİRHAN ŞAHİN - BURAK DUYSAK - HALİS AYDIN

INTRODUCTION

The interest in image capture and processing is increasing day by day, and the application areas of image capture and processing are expanding. Likewise, the popularity of "Field Programmable Gate Arrays (FPGA)" hardware is increasing day by day. FPGAs can perform multiple tasks simultaneously thanks to their parallel processing capabilities.For this reason, it is often preferred in applications that require high speed.

In this project, it is aimed to design a compact image capture device using FPGA and to display the real-time image captured by the camera in computer environment over Ethernet.

Application Areas

This capture card can then be developed and used for image processing. Because, thanks to its parallel processing speed and the power of FPGA innovation, this project can be a building block for image processing or machine learning projects. Image processing algorithms are used in many areas such as security systems, health sector, radar, satellite systems. Some image processing algorithms can be designed on FPGA-based development boards, such as changing color in the image in real time, morphological on and off, red object tracking, skin color recognition, applying a sobel filter to the image.

Digital Design

All digital designs are based on Verilog and VHDL codes.

The analog camera was used with the ADV7180 module, which was used as an analog to digital converter. Inside the FPGA fabric, camera decoder, color conversion algorithms, JPEG Encoder algorithm, UDP wrapper, and Ethernet Controller is applied. The 64 Mb CMOS SDRAM is used for frame buffering.

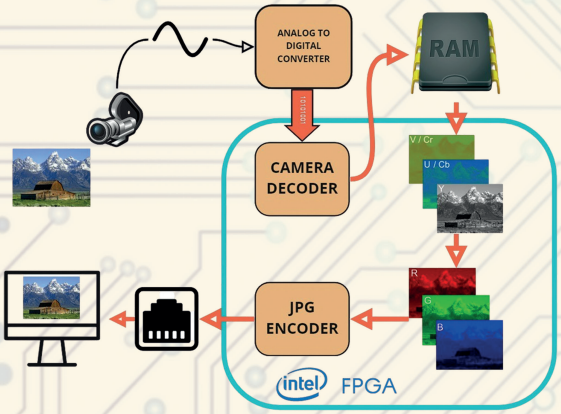
JPEG Encoder IP Core

The input image to JPEG Encoder is 640x480 24-bit RGB color. 7.3 ms processing time @ 100 MHz clock (2.3 clock cycles per input sample)

Input file size = 921 kB. Output file size = 44 kB (depends on image)

Ethernet IP Core

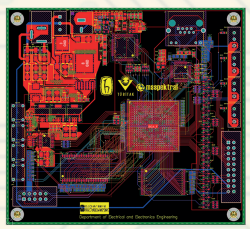
The Ethernet IP Core is a 10/100 Media Access Controller (MAC). It consists of a synthesizable Verilog RTL core that provides all features necessary to implement the Layer 2 protocol of the Ethernet standard. At full blast, the UDP wrapper is able to transmit up to 8 megabytes per second.

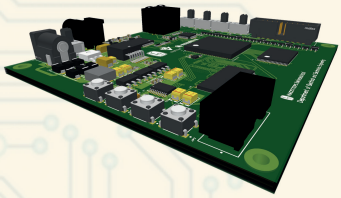


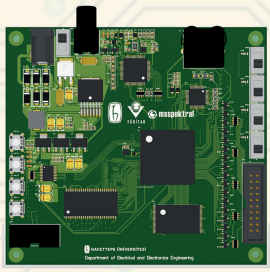
Hardware Design

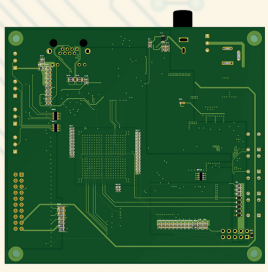
Based on the design requirements, our project's schematic designs and PCB layout are designed using Altium Designer software.The images show the PCB layout of the system designed for hardware implementation.

The designed system consists of many building blocks. These are 64Mb-SDRAM, 32Mb-FLASH MEMORY,Ethernet controller and Multiformat SDTV video decoder. Our design features EP2C35F484C8 FPGA Cyclone® II Family processor.The designed PCB layout is an 8-layer board design with dimensions of 100mmx110mm.









Acknowledgements

This project was completed within the context of ELE401-402 Graduation Project courses in Hacettepe University, Faculty of Engineering, Department of Electrical and Electronics Engineering.

We thank Prof.Dr. Ali Ziya Alkar for his invaluable contributions to our project.

We would like to thank TÜBİTAK for providing a great opportunity with the "2209-A University Students Research Projects Support Program" and MS Spectral for their financial support.